REMARKS

Claims 1-14 and 16-34 are pending, with claims 1, 16, 18, 20, 21, 27, 30 and 33 being independent. Claims 27-34 are newly added and are supported, for example, at page 9, lines 8-13, and by Fig. 1. Claim 15 was previously cancelled. No new matter has been added.

Claims 1-14, 21-22 and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 5,250,931 to Misawa et al. (Misawa) in view of U.S. Patent No. 5,818,068 to Sasaki et al. (Sasaki) and U.S. Patent No. 5,550.070 to Funai et al. (Funai). Claims 16-19, 23, and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sasaki in view of U.S. Patent No. 5,888,857 to Zhang et al.(Zhang). Claims 20 and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sasaki in view of U.S. Patent No. 5,959,599 to Hirakata (Hirakata).

Regarding the rejection of independent claim 1 as being unpatentable over Misawa in view of Sasaki and Funai, Applicant respectfully submits that claim 1 is neither disclosed nor suggested by any proper combination of the cited references.

As pointed out in Applicant's previous response, independent claim 1 recites a limitation that, "... the pixel matrix circuit, the driver circuit and the logic circuit are disposed over a same substrate, wherein the pixel matrix circuit, the driver circuit, and the logic circuit are constituted by a plurality of thin film transistors ..." The Office Action acknowledges (see paragraphs bridging pages 3 and 4 of the Office Action) that Misawa fails to disclose this limitation. However, the Office Action states that Misawa discloses positioning the driver circuit and pixel matrix circuit on the same substrate, and that "(t)herefore, it would have been obvious to allow the logic circuits to as well be included on the substrate along with the driving circuitry." The Office Action goes on to state that Sasaki discloses such a logic circuit.

In refuting the validity of this rejection, Applicant respectfully requests that the Examiner re-read the Background section of the present application (pages 1-3). In that section, Applicant specifically refers to Misawa and discusses its teaching of including (only) a driver circuit and pixel matrix circuit on a same substrate (see Application, page 1, lines 20-25). Further, Applicant refers to the concept of including a logic circuit (comprising TFTs), which is

conventionally external to an active matrix display, on the same substrate. Applicant goes on to discuss reasons why such a construction did not conventionally exist at the time of filing. For example, the application states at page 1, lines 10-13, that "...it is difficult to constitute an electric circuit requiring high frequency driving, such as a logic circuit, by TFTs using presently employed silicon thin films." The application goes on to elaborate on several reasons and examples as to the difficulties of employing pixel matrix circuits, driver circuits, and logic circuits, each comprising TFTs, on a same substrate (see Application, pages 2-3).

In light of Applicant's disclosure, then, the conclusory statement of the present Office Action that "... it would have been obvious to allow the logic circuits (allegedly of Sasaki) to ... be included on the substrate along with the driving circuitry (of Misawa)" seems particularly ill-suited to serve as the basis of a prima facie case of obviousness under 35 U.S.C. 103(a). In particular, such a prima facie case of obviousness requires, for example, "a reasonable expectation of success" to be established by the Examiner. Particularly in the field of semiconductor devices, there are a host of issues that may prevent a certain number or type of circuits from being included together, on the same substrate or otherwise. For example, consideration must be made of the types of circuits involved, the materials used, the fabrication process(es), and so on. That is, even acknowledging for arguments sake that it is desirable to include more and more circuits on a single chip or substrate, this fact alone does not mean that one of ordinary skill in the art would have reasonably expected to do so at the time of the invention.

Moreover, MPEP 2142 states that when, as is the case here, evidence has been provided as to non-obviousness, "... such as any evidence in the specification ... (then) ... with regard to rejections under 35 U.S.C. 103, the examiner must provide evidence (in rebuttal) which as a whole shows that ... a prima facie case of obviousness ... is more probable than not."

Accordingly, Applicant respectfully requests that the Examiner provide evidence supporting the above-rejection under 35 U.S.C. 103 based on Misawa and Sasaki, where such evidence considers and rebuts each one of the points of evidence presented in the present application and referred to above. In this regard, Applicant notes that the I/O port of Sasaki,

referred to by the Office Action as the claimed logic circuit, is included in a **driver** circuit of Sasaki, and therefore does not disclose the logic circuit as recited in claim 1 (much less that such a logic circuit be included on a substrate with the claimed driver circuit and pixel matrix circuit).

Unless and until such evidence is presented by the Examiner, Applicant respectfully submits that independent claim 1 is allowable for at least the above reasons, so that dependent claims 2-14 and 22 are allowable for at least the same reasons.

Further, each of the remaining independent claims 16, 18, 20, and 21 recite a logic circuit that is formed over the same substrate as a recited pixel matrix circuit and driver circuit, where the logic circuit, pixel matrix circuit, and driver circuit are formed of thin film transistors. Since (as discussed above) the cited references neither disclose nor properly suggest these features, as claimed, and pending the Examiner's production of evidence to the contrary, Applicant submits that independent claims 16, 18, 20, and 21 (as well as dependent claims 17, 19, and 23-26) are allowable.

In particular, with reference to independent claims 16 and 18, Applicant notes that the rejection of these claims based on Sasaki in view of Zhang (see paragraph 3 at pages 6-7 of the Office Action) does not even address the issue of forming pixel matrix, driver, and logic circuits comprising thin-film transistors on a same substrate, as recited in independent claims 16 and 18. Similarly, the rejection of independent claim 20 based on Sasaki in view of Hirakata does not address the issue of this claim limitation, as recited in independent claim 20 (moreover, Applicant submits that neither Sasaki nor Hirakata teach gate insulating films with different thickness formed on a substrate, as recited in claim 20).

Moreover, dependent claim 2 recites that "... crystal lattices of the plurality of rod-shaped crystals are continuous within each of the active layers so that there is no barrier for carriers within each of the active layers." Applicant notes that even if the silicon crystal of Funai, which is applied to claim 2, has no grain boundaries in one direction (see, e.g., column 10 line 11-15 of Funai et al.), as just recited, claim 2 requires that there be no barrier for carriers within each of the active layers.

Further, claims 8 and 9 require that an active layer contain an element selected from Cl, F, and Br, whereas the Office Action, at page 5, refers to Sasaki as teaching nickel, iron, cobalt, palladium, or platinum. In particular, with reference to claim 9, the claimed element is required to be one of Cl, F and Br, not nickel, as set forth in the Office Action.

With reference to claims 11-13, Applicant notes that the "storage capacitor" in claim 11 is recited as being formed between a connect wiring and a black mask. In contrast, the capacitor of Misawa is formed between a liquid crystal 96 and an electrode 92 (See Fig. 3B and column 7 line 30-35 of Misawa et al.).

Since all pending claims are in condition for allowance, such action is requested in the Examiner's next official communication.

A check in the amount of $1592.00 ($402.00 for extra claim fees, $420.00 for Two-Month Extension and $770.00 for RCE Filing Fee) is enclosed. Please apply any additional charges or credits to deposit account 06-1050.

Respectfully submitted,

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